High Efficiency 1.2MHz, 30V BOOST

FEATURES

- 2.5V to 5.5V Input Voltage
- 1.23V Feedback Voltage
- 1.2MHz Fixed Switching Frequency
- Internal 0.6A Switch Current Limit
- Internal Compensation
- Thermal Shutdown
- Available in a 5-pin SOT-23 package

APPLICATIONS

- Camera Flash White LED
- PDA LED back light
- Digital still cameras

GENERAL DESCRIPTION

The EC3750 is a step-up converter. Its 1.23V feedback voltage reduces power loss and improves efficiency.
Optimized operation frequency can meet the requirement of small LC filters value and low operation current with high efficiency. Internal soft start function can reduce the inrush current. Tiny package type provides the best solution for PCB space saving and total BOM cost.

TYPICAL APPLICATION

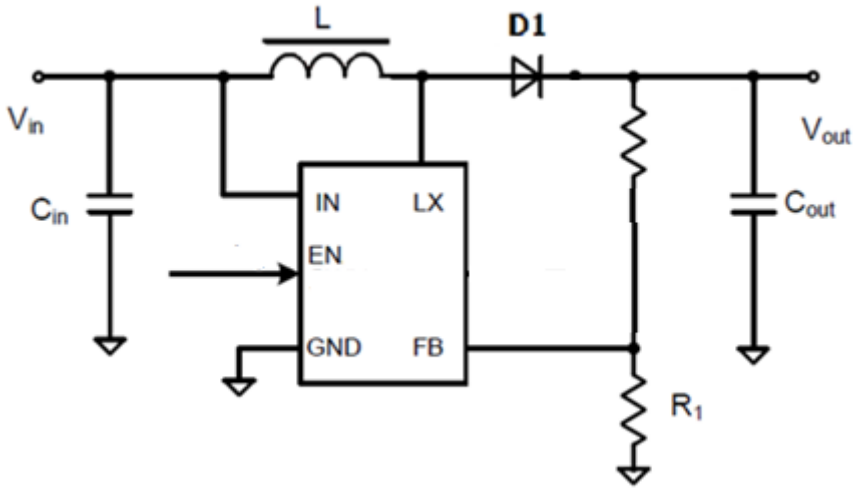
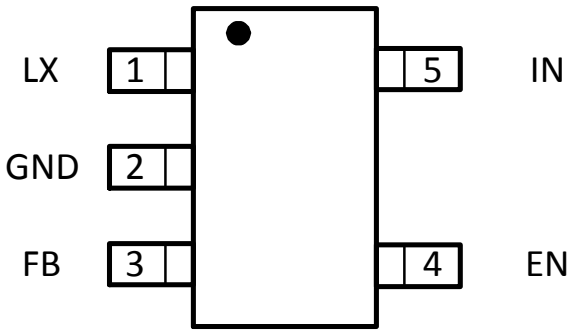


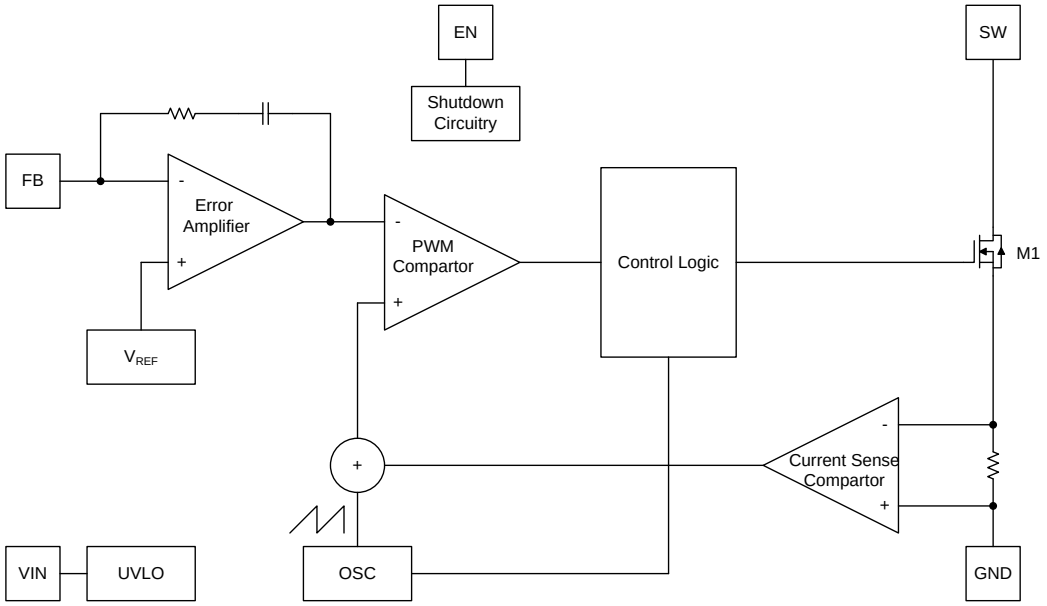
Figure1. Basic Application Circuit

PACKAGE & PIN DESCRIPTION



PIN	NAME	FUNCTION
1	LX	Power Switch Output. LX is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to LX. LX can swing between GND and 30V.
2	GND	Ground Pin
3	FB	Feedback Input. The FB voltage is 1.23V. Connect a resistor divider to FB.
4	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup.
5	IN	Input Supply Pin. Must be locally bypassed.

SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	ABSOLUTE MAXIMUM RATINGS	UNIT
V_{IN}, V_{EN}	-0.3 to 6	V
V_{SW}	-0.3 to 30	V
All Other Pins	-0.3 to 6	V
Continuous Power Dissipation(T_A=+25℃)	0.6	W
Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	
Lead Temperature	260	°C
Storage Temperature	-65 to 150	°C
Thermal Resistanceθ_{JA}	250	°C /W
Thermal Resistanceθ_{JC}	130	°C /W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RECOMMENDED	UNIT
Supply Voltage V_{IN}	2.5 to 5.5	V
Output Voltage V_{OUT}	V_{IN} to 30	V
Operating Junction Temp.(T_J)	-40 to 125	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current(Shutdown)	I_{IN}	V_{EN}=0V		0.1	1	μA
Quiescent Current		V_{FB}=1V,switch		0.15	0.3	mA
SW Leakage		V_{SW} = 20V			1	μA
SW On Resistance				400	650	mΩ
Operating Input Voltage			2.5		5.5	V
Current Limit	I_{LIMIT}	V_{IN}= 4V,Duty cycle=50%		0.6		A
Oscillator Frequency	f_{SW}			1.2		MHz
Maximum Duty Cycle	D_{MAX}			90		%
Feedback Voltage	V_{FB}		1.21	1.23	1.25	mV
FB Input Bias Current		V_{FB}=1V	-50	-10		nA
EN Threshold	V_{EN}			1		V
Thermal Shutdown				160		°C

Detailed Design Procedure

External Components Selection

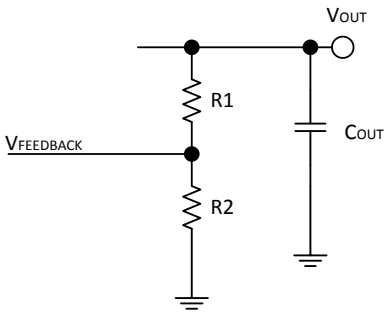
EC3750 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FEEDBACK} \times \frac{R1 + R2}{R2}$$

Select *R1* value around 50kΩ

$$R2 = R1 \times \frac{V_{FEEDBACK}}{V_{OUT} - V_{FEEDBACK}}$$

Where *VFEEDBACK* As 1.23V



Inductor Selection

The EC3750 boost converter can utilize small surface mount and chip inductors due to the fast 1.2MHz switching frequency. Inductor values between 2.2µH and 10µH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10µH will increase size while providing little improvement in output current capability. The minimum boost inductance value is given by:

$$L > \frac{V_{IN} \times (V_{OUT} + V_{DIODE} - V_{IN})}{F_S \times I_{RIPPLE} \times (V_{OUT} + V_{DIODE})}$$

Where

- *IRIPPLE*：Peak-to-Peak inductor current
- *VIN*：Input voltage
- *VOUT*：Output voltage
- *VDIODE*：Output diode Forward Voltage
- *FS*：Switching frequency, Hertz

The inductor current ripple is typically set for 20% to40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DCR(series resistance of the winding) to reduce the I^2R power losses, and must not saturate at peak inductor current levels. Molded chokes and some chip inductors usually

Input and Output Capacitor Selection

The internal loop compensation of the EC3750 boost converter is designed to be stable with output capacitor values of 10µF or greater. Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 10µF to 22µF output capacitor is sufficient for most fixed frequency applications. For applications where Burst Mode operation is enabled, a minimum value of 22µF is recommended. Larger values may be used to obtain very low output ripple and to improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Case sizes smaller than 0805 are not recommended due to their increased DC bias effect.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 22µF input capacitor connected to inductor is sufficient for most applications. Larger values maybe used without limitations. For applications where the power source is more than a few inches away, a larger bulk decoupling capacitor is recommended on the input to the boost converter.

Output Diode Selection

A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

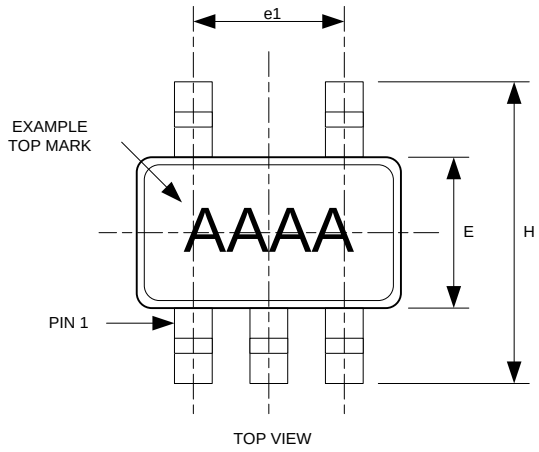
Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

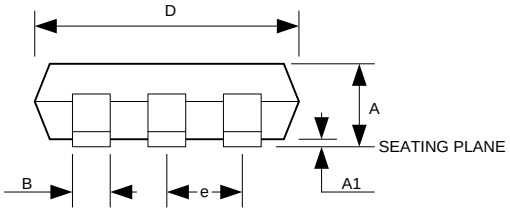
1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the *CIN* input capacitor, to the regulator *VIN* terminal, to the regulator *SW* terminal, to the inductor then out to the output capacitor *COUT* and load. The second loop starts from the output capacitor ground, to the regulator *GND* terminals, to the inductor and then out to *COUT* and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the *VIN* terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to *GND*. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The *SW* terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the *SW* terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the *GND* pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the *FB* terminal. The feedback trace should be routed away from the *SW* pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

PACKAGE INFORMATION

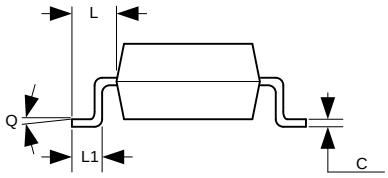
SOT23-5



TOP VIEW



FRONT VIEW



SIDE VIEW

5LD SOT-23 PACKAGE OUTLINE DIMENSIONS

Dimension	Min.	Max.
A	1.05	1.35
A1	0.04	0.15
B	0.3	0.5
C	0.09	0.2
D	2.8	3.0
H	2.5	3.1
E	1.5	1.7
e	0.95 REF.	
e1	1.90 REF.	
L1	0.2	0.55
L	0.35	0.8
Q	0°	10°

NOTE:
1.DIMENSIONS ARE IN MILLIMETERS
2.DRAWING NOT TO SCALE
3.DIMENSIONS ARE INCLUSIVE OF PLATING
4.DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR